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Enhancing the Dorsal Side of Fingers Using An Image Enhancement Technique with FPGA Output Comparison

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Abstract

Most of the image enhancement techniques are implemented on CPU and GPU, but there is limited implementation on the FPGA platform. This paper presents a work on an enhancement technique called Histogram Equalization, HE for finger-knuckle images. This project is divided into three phases, which are image acquisition, image enhancement, and evaluation. For image acquisition, a USB webcam is set up as the acquisition device to acquire the image of fingers. For image enhancement, the Histogram Equalization (HE) method is chosen due to the less complex algorithm, especially when evaluating the performance on the FPGA platform. Two processing platforms are considered to complete the study, which are desktop computers that use MATLAB programming and the FPGA DE1-SoC platform. A comparison of the results is carried out between these two processing platforms, where it is found that the results for both platforms have shown identical output in terms of PSNR, which achieved a value of 13.43 dB and MSE with 0.0454.

Keywords: Finger-Knuckle-Print (FKP), FPGA, Histogram Equalization (HE), Image Enhancement, Verilog HDL.

Introduction

Biometric authentication has received significant attention due to its high level of assurance and security. FKP utilizes the crease and texture patterns on the finger knuckles in the recognition process. The global biometric system market is projected to grow from USD 42.9 billion in 2022 to USD 82.9 billion by 2027, indicating the increasing significance of biometric authentication[1]. Image enhancement techniques such as Histogram Equalization (HE) have also been explored to improve the accuracy of FKP recognition[2]. For the portable finger vein recognition system based on Xilinx XC7A75T and ARM Cortex-M3 kernel FPGA using System on Chip (SOC) solution and achieved greater than 97% recognition accuracy[3]. An FPGA-based parallel fingerprint matching with early jump-out control system proposed to accelerate the matching process[4]. A fingerprint matching system using global matching algorithm by implementing Coarse-Grained architecture achieved 9.63 million matches per second[5].

Researchers have focused on developing efficient algorithms for feature extraction and recognition[6,7]. Even though various existing works showcase the implementation of HE, there are a number of limitations to them. Most of the image enhancement techniques are implemented on CPU and GPU by using MATLAB and Python. Hence, FPGA-based systems need to be explored to achieve low latency, high throughput, and optimized power efficiency. There are limited previous works on the implementation of Histogram Equalization on the FPGA platform by using Verilog HDL. Aside from having a clear image for the FKP recognition process, a standard image of the dorsal side of the finger acquisition system is very important. A typical image acquisition device should be included with a camera from a fixed distance and try to avoid misplacement of the fingers. The main contributions of this research work are summarized as: (i) An acquisition system is developed that can capture multiple images of dorsal side fingers at once. (ii) The image enhancement technique applied using MATLAB, where this approach aims to evaluate the effectiveness of the algorithm in terms of showing the appropriate image output after the enhancement process. On the FPGA platform, the approach is suggested to evaluate and compare the result when the same algorithm is applied on a hardware-based platform. (iii) Experiments are performed using a real-time self-collected dataset and compared the results of image enhancement from MATLAB with the FPGA platform for the HE algorithm.

Histogram Equalization (HE) is widely used in various fields, including thermal imaging, speech recognition, and radiology. In HE, the difference between objects and background is enlarged by expanding the pixels with significant gray value occurrences to adjacent gray level pixels, and the pixels with minor gray quantity occurrences are squeezed. Authors applied a parallelism approach for local histogram equalization using FPGA and achieved faster image enhancement compared to other conventional methods[8]. Alsuwailem and Aishebeili introduced a unique FPGA-based design for real-time histogram equalization. The design employs non-traditional approaches to compute histogram statistics and equalization in parallel. Counters are used in conjunction with a decoder explicitly created for this reason. The hardware has a low development cost and is faster and more versatile. For a 256 × 256 image, the total time required to execute histogram equalization is 0.262 ms[9].

Table 1 shows a summary of the comparison of related works in terms of the strengths and limitations of the image acquisition system. In contrast, Table 2 shows an overview of the comparison of related works in terms of strengths and limitations for image enhancement on FPGA.

Table 1. Comparison of different image acquisition systems

Methodology	Strength	Limitations
Wooden case with camera [10]	High efficiency in collecting many images	Misplacement and finger rotation may occur
A finger-knuckle-print acquisition device with a triangular block[11]	Prevent misplacement and wrong pose of finger	High cost and low efficiency in collecting many images
Dorsal finger crease image collection with Logi-Tech pro-webcam[12]	User friendly for image acquisition	Low cost and requires efficient pre-processing techniques

Table 2. Comparison of related works on image enhancement on FPGA

Methodology	Strength	Limitations
HE, AHE, CLAHE on CPU[13]	Shows that CLAHE is the most suitable technique in general condition	Lower performance compared to FPGA
Brightness manipulation, threshold operation, and invert operation on FPGA[14]	Implement on FPGA by Verilog HDL	Not an image enhancement technique that improves the contrast of the image
HE on Zynq FPGA[15]	Implement on FPGA	Rely on Vivado high level synthesis tool
CLAHE on FPGA[16]	Speedup of about 3.67 times for 512×512 images and a speedup of about 2.98 times for 1920×1080 images in FPGA.	Rely on HLS

Materials and Methods

In this section the proposed methodology is discussed which involves three stages consisting of: (i) development of dorsal side fingers image acquisition, (ii) image enhancement, (iii) and performance evaluation. The overall process of the system is summarized as shown in the flowchart in Fig. 1. In the first stage, the acquisition system is developed with an appropriate camera distance between the camera and the plate for locating the fingers. At this stage, a Python module is developed to capture dorsal side finger images and extract the region of interest. In the second stage, image enhancement techniques are employed and coded using MATLAB. On the FPGA platform, the image is first converted into HEX format and uploaded to the FPGA board for performing the HE algorithm. The output of the processed HE, which is also in HEX format, is exported to MATLAB for producing the image output. The last phase involves evaluating the enhanced images by calculating MSE and PSNR and comparing results between MATLAB and FPGA implementations.

Hardware and software setup

The hardware resources used in this project are a USB webcam and a DE1-SoC development board. A 2K HD webcam with panoramic high definition 2560 × 1440p resolution is used. The image sensor used is CMOS, while the frame rate is 30fps. This camera is used in the image acquisition system to capture the image of the dorsal side of the fingers. The proposed system is developed on an FPGA board named the DE-SoC development board. The FPGA device in this board is Cyclone V SoC 5CSEMA5F31 device. The software resources used in this project are Python, MATLAB, ModelSim, and Quartus Prime. Python module with OpenCV library is used in the image acquisition system to control the webcam and pre-process the images captured. MATLAB is used to verify the algorithm before implementing it on the FPGA board as it is relatively simple compared to coding in Verilog. Model Sim is used to verify the Verilog modules as the internal signal of the system can be observed in the waveform. Quartus Prime is used to design and program the algorithm onto the FPGA board. FPGA is implemented using Verilog due to fast processing in term of algorithm. Therefore, with finger knuckle print authentication that need fast response, it contributes better platform in implementing finger knuckle authentication system.

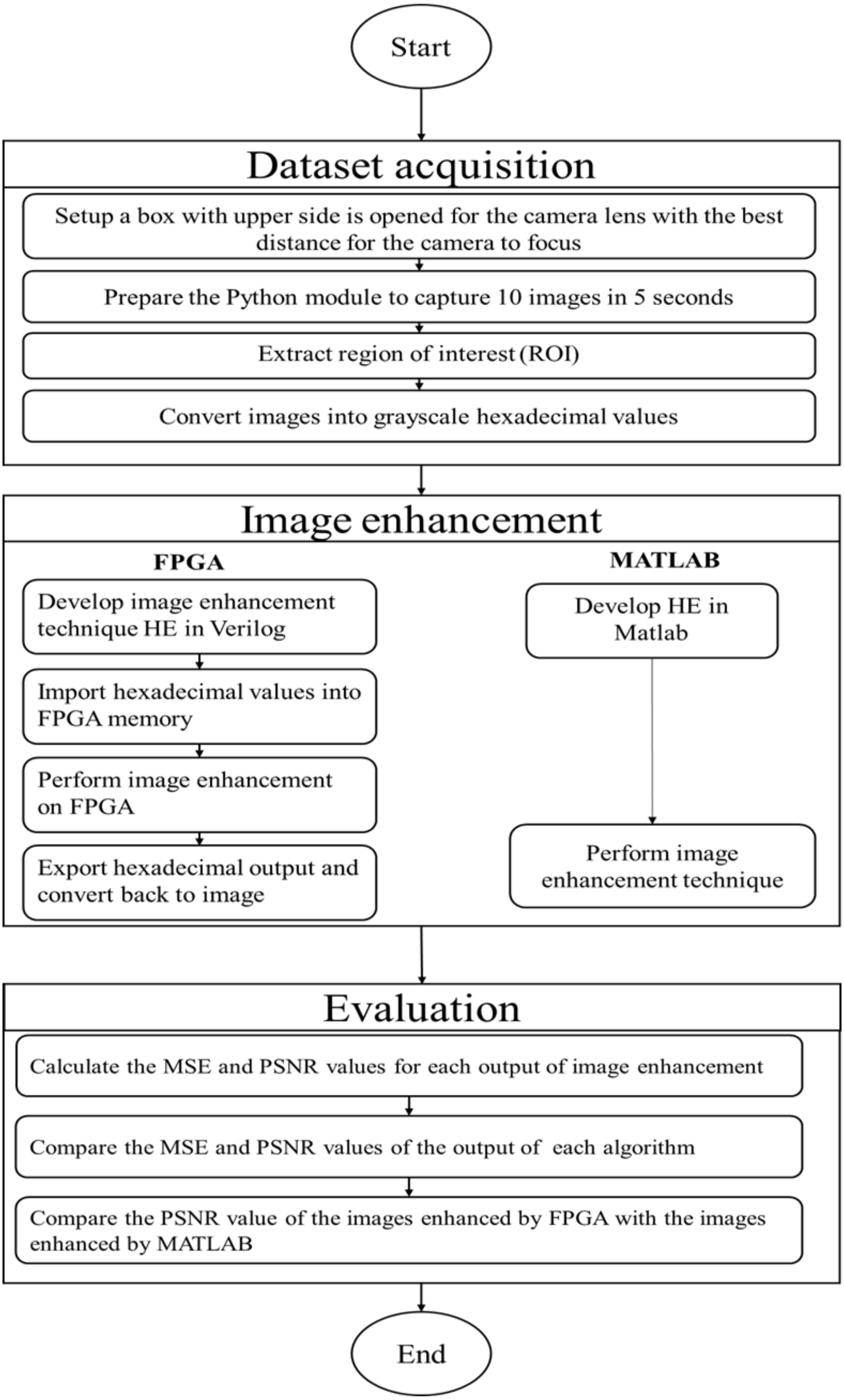

Start
Dataset acquisition
Setup a box with upper side is opened for the camera lens with the best distance for the camera to focus
Prepare the Python module to capture 10 images in 5 seconds
Extract region of interest (ROI)
Convert images into grayscale hexadecimal values
Image enhancement
FPGA
Develop image enhancement technique HE in Verilog
Import hexadecimal values into FPGA memory
Perform image enhancement on FPGA
Export hexadecimal output and convert back to image
MATLAB
Develop HE in Matlab
Perform image enhancement technique
Evaluation
Calculate the MSE and PSNR values for each output of image enhancement
Compare the MSE and PSNR values of the output of each algorithm
Compare the PSNR value of the images enhanced by FPGA with the images enhanced by MATLAB
End

Figure 1. Flowchart of the proposed work

Image acquisition

In the first stage, the image acquisition device is built to capture the image of the dorsal side of the fingers. The camera lens is then placed on the box that has its upper side open. On the lower side of the box, a guideline is drawn so that the finger can align the finger-knuckle with it. Fig.2 shows the entire image acquisition device with the webcam and the procedure. A Python module controls the webcam to capture images. For this study, ten images are captured with limited rotation of the finger to obtain the correct location of the region of interest.

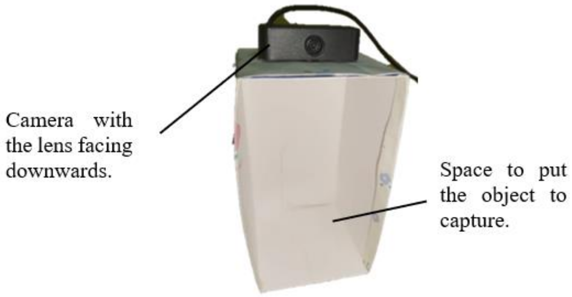

Camera with the lens facing downwards.
Space to put the object to capture.

Figure 2. Proposed Image acquisition device

Image enhancement

The images are converted into grayscale before performing the image enhancement algorithms. For image enhancement implementation on FPGA, a Verilog code for the HE is written, in which Fig. 3 shows the block diagram of HE modules after performing the algorithm. In this study, Verilog is written directly without using any existing modules. Compared to the previous study, most of the research has used VHDL modules using HDL coder or HLS. In implementing the HE on FPGA, the intel format hex is uploaded into the RAM of the FPGA board. The image data in HEX format is processed with the Histogram Equalization Verilog module. The processed data is also in hexadecimal value, and the data is written in a text-based format file. The text file is then transferred into MATLAB for converting it into an image again. The output image is then compared to the original image. The intel hex format file is imported into the FPGA RAM by using the In-System Memory Content Editor. To perform the image enhancement on FPGA, the FPGA board is connected to the desktop computer. The SRAM Object File as .sof file is selected and programmed to the board. The image data is imported to the RAM1. The second RAM (ram2) is then selected and acquires the data continuously from the RAM to the content editor. Then, the HE algorithm is performed. When the process of HE is finished, the new data values are shown in the memory content editor. The data is the enhanced image content that is ready to be exported, which is also in a hex file. The extracted hexadecimal values are then processed to convert into images in the MATLAB platform.

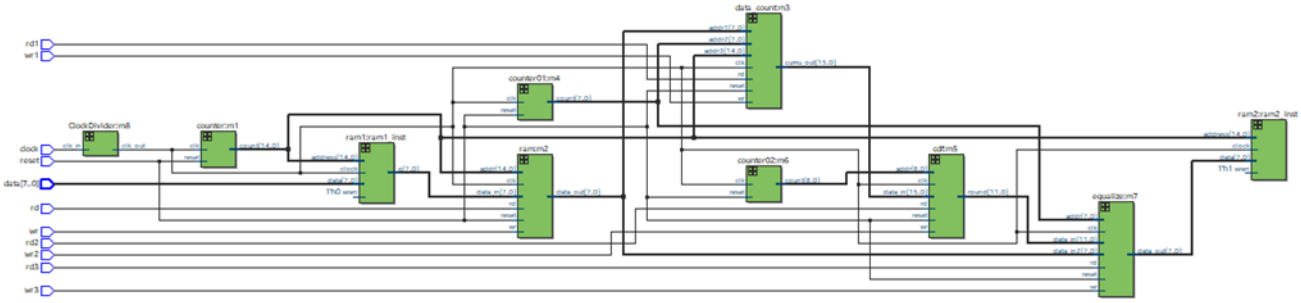


Figure 3. Block diagram of image enhancement using FPGA

Performance evaluation metrics

The data analysis is carried out in the evaluation phase for the result of the image enhancement process. The image enhancement algorithms are evaluated by calculating the Peak signal-to-noise ratio (PSNR) and Mean Square Error (MSE). In the evaluation phase, the MSE and PSNR modules are written in MATLAB code. The PSNR value is calculated by using Eq. 1:

$$PSNR = 10\, log_{10}\left(\frac{R^2}{MSE}\right) \qquad 1$$

R is the maximum variation in the input image data. For example, if it has an 8-bit data type, R is equal to 255. MSE is the mean square error, which is calculated by Eq. 2:

$$MSE = \frac{\sum_{M,N}[I_1(m,n) - \ I_2(m,n)]^2}{M,N} \qquad 2$$

Here, I_1 is the original image, I_2 is the enhanced image, while M and N are the height and width of the image, m and n represent the pixel of the image in rows and columns.

Results and Discussion

This section discusses the assessment that has been made from the discussed methodology. For the ROI determination, only manually performed it by setting the coordinated for four ROI points, as shown in Table 3. After that, the ROI image is resized into 151×133 pixels purposely to reduce the computation time, particularly on the FPGA platform. An example of the image after performing the ROI process is shown in Fig. 4.

Table 3. Coordinate values for region of interest (ROI) points

ROI Points	Coordinates
x_1	370
x_2	432
y_1	260
y_2	350

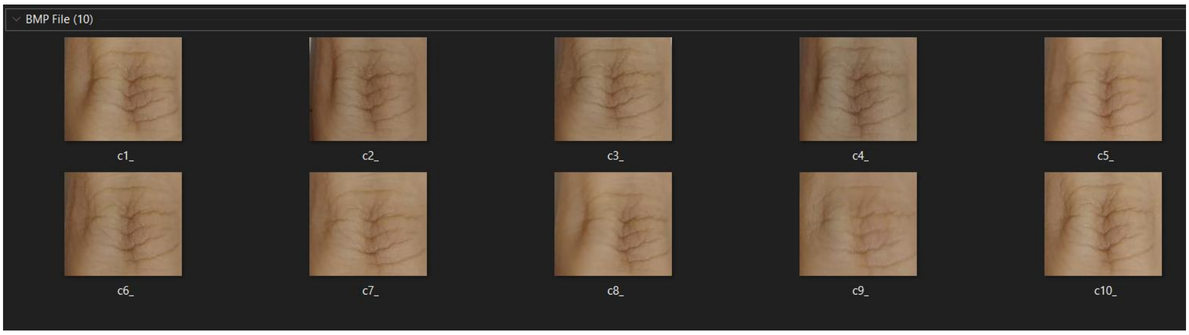
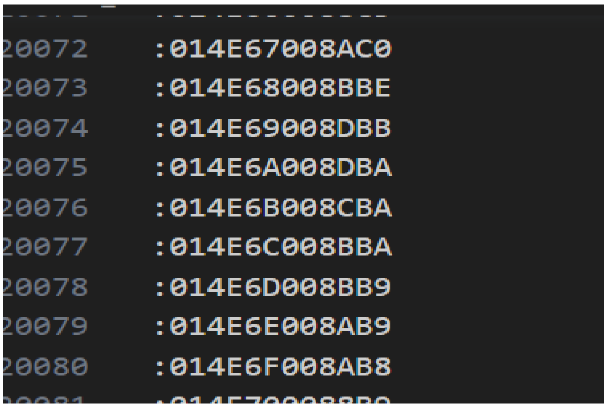


Figure 4. Sample images of the extracted ROI

The ROI is then converted into grayscale and then converted into hex data by using the Python PIL library. The output hexadecimal values are stored in a new file with the image filename plus 'hex' in a text file (e.g., c1_hex.txt). There are a total of 20083 lines to store the information of the image as the image size is 151 × 133 pixels. The output text file is then loaded into the Python module again to convert it into Intel hex format, as in Fig. 5.



```
20072   :014E67008AC0
20073   :014E68008BBE
20074   :014E69008DBB
20075   :014E6A008DBA
20076   :014E6B008CBA
20077   :014E6C008BBA
20078   :014E6D008BB9
20079   :014E6E008AB9
20080   :014E6F008AB8
```

Figure 5. Intel hex format file Image enhancement on FPGA

In FPGA, Model Sim is used to verify the modules before implementing them on the FPGA board. Fig. 6 shows the simulation result of the test bench module of HE. The first input is set, reset, and wr as 1, and the rest remain 0. This activates the process of moving the input data into a RAM with a new address that cancels the delay. The second set of input is to set, reset, rd, and wr1 to 1 to activate the data count module. Then, reset, rd1, and wr2 are set to 1 to calculate the cumulative value. The following input is to set reset, rd2, and wr3 to 1 to perform the calculation of CDF. The last set of information is to set reset, rd, and rd3 to 1 to map the equalized data to the pixel of the image. The HE modules are validated through this simulation. The visual comparison of the enhanced image on FPGA with the original image is shown in Fig. 7.

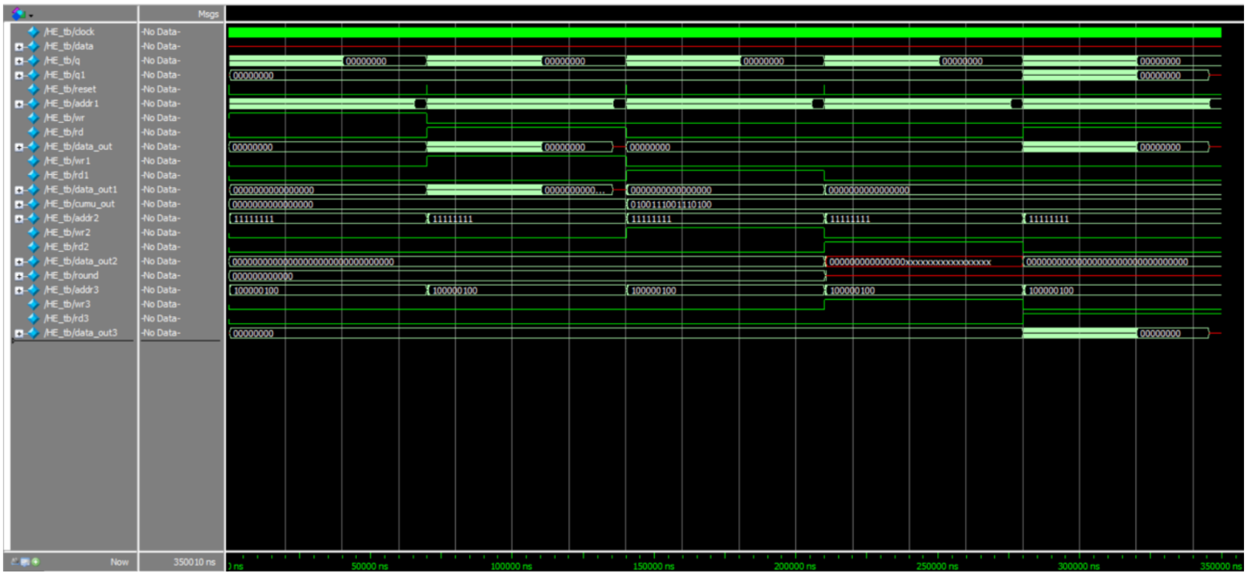


Figure 6. FPGA Simulation result

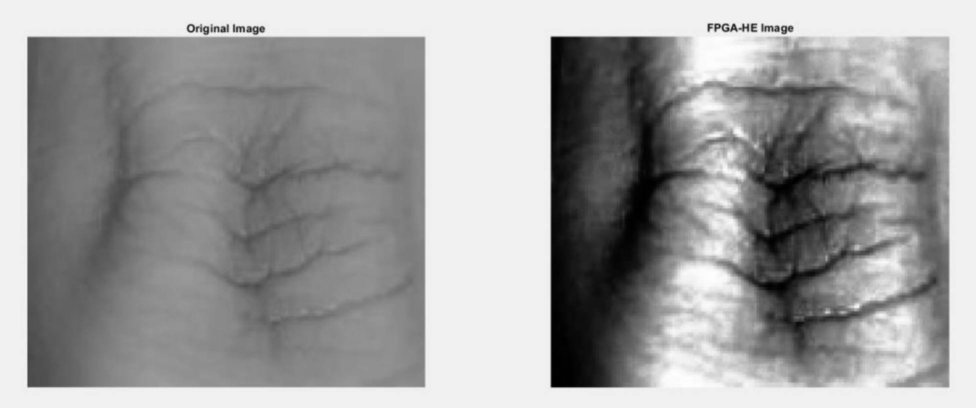


Figure 7. Visual comparison of FPGA enhanced image with the original image

As shown in Fig. 7, the image is enhanced, and the finger-knuckle-print can be seen more clearly compared to the original image. In short, the image enhancement algorithm HE is successfully being implemented on the FPGA board. It is found that the quality of the image after performing the HE algorithm is improved. However, there are also some limitations to this methodology. By using on-board memory IP in Quartus, the data stored in the RAM is read address by address. This may require more processing units in designing the Verilog module if a more complex algorithm than HE is chosen to be processed on FPGA.

Image enhancement on MATLAB

In this phase, a similar HE algorithm is performed and written in MATLAB. The original images are loaded into the modules and are changed into grayscale images. The output image is saved as a bitmap image and displayed in a subplot together with the original grayscale image, as in Fig. 8 for the HE method.

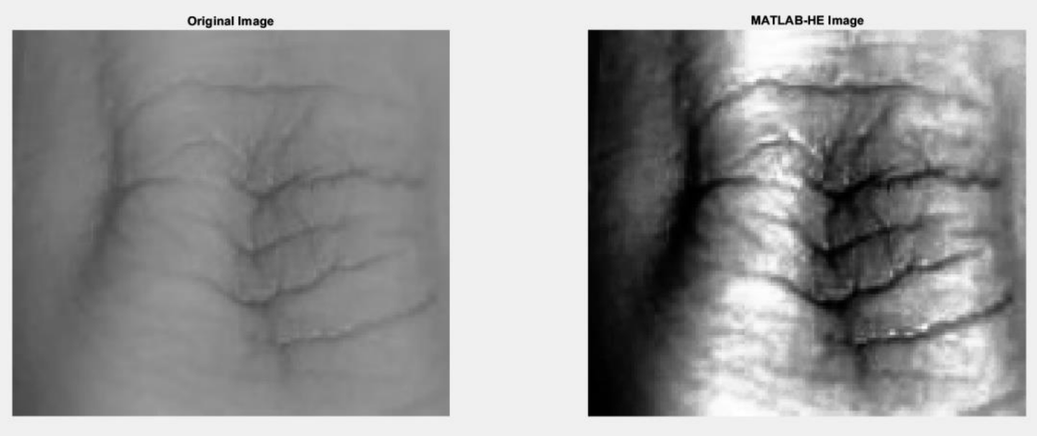


Figure 8. Comparison of HE image with the original image

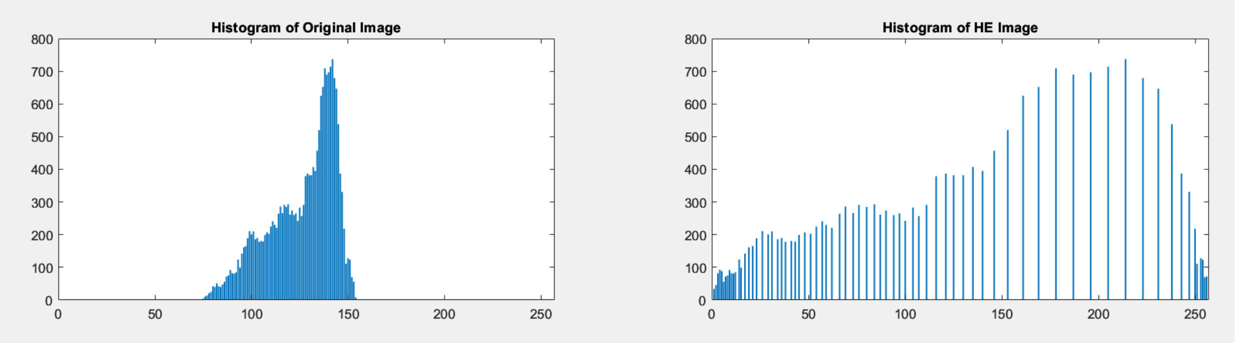


Figure 9. Histogram of the original image and HE image

Compared to the original image, the finger-knuckle-print is more apparent where it can be seen that after applying HE, the histogram of the image has a more uniform distribution of pixel intensities, as shown in Fig. 9. There is a broader range of intensities being utilized as the peaks and valleys have been flattened. The redistribution of the pixels enhanced the overall contrast of the image and improved the visual appearance of the image. In Fig. 9, the histogram presents a more balanced distribution of the pixel intensities, resulting in a better utilization of the available intensity range. The histogram also displays a more significant peak, indicating the presence of distinct intensity levels in the image.

In the phase of evaluation, the values of MSE and PSNR are compared for each image enhancement algorithm on each platform. The higher the PSNR value, the better the quality of the image is preserved.

Table 4. Table of MSE and PSNR values for each output image

Image enhancement	MSE	PSNR (dB)
FPGA - HE	0.0454	13.43
MATLAB - HE	0.0454	13.43

As shown in Table 4, the MSE value of the FPGA implementation of HE and the MSE value of MATLAB implementation are the same, which is 0.454. The PSNR value for the FPGA implementation is also the same as in MATLAB (13.43dB). This verified that HE can be implemented on FPGA by using proper Verilog modules instead of using HLS.

Conclusion

In conclusion, the research objectives of this project have been achieved. A dorsal side of the finger image with different image enhancement methods has been applied and assessed on both MATLAB and the FPGA platform. From the result, it is found that the chosen technique can be used particularly on the

FPGA platform with appropriate consideration in terms of converting the image into a specific format that can be processed on the FPGA platform without using the HLS. The current research work focused only on image enhancement techniques with FPGA implementations and in future the plan is to develop a complete FPGA based biometric system from data collection to final matching stage with larger database.

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Authors' Declaration

- Conflicts of Interest: None.
- We hereby confirm that all the Figures and Tables in the manuscript are ours. Furthermore, any Figures and images, that are not ours, have been included with the necessary permission for re-publication, which is attached to the manuscript.
- No animal studies are present in the manuscript.
- The images used in this study are acquired through approval ethical protocol with the study protocol code USM/JEPeM/21100657.
- Ethical Clearance: The project was approved by the local ethical committee at Universiti Sains Malaysia, Malaysia.

Authors' Contribution Statement

T. S. H., A. N. A. and I. R. designed and conceptualized the study. T. S. H. performed the experiments for data collection, image enhancement and performed analysis. T. S. H. and I. R. performed simulations experiments. T.S.H. and I.R. wrote the paper with input from all authors. I.R., and A.N.A. reviewed and edited the paper.

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تحسين الجانب الظهري للأصابع باستخدام تقنية تحسين الصورة من خلال مقارنة مخرجات FPGA

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الخلاصة

يعرض هذا البحث عملاً على تقنية تحسين تسمى معادلة الرسم البياني، HE لصور مفصل الإصبع. وينقسم هذا المشروع إلى ثلاث مراحل، وهي الحصول على الصور، وتحسين الصورة، والتقييم. للحصول على الصور، يتم إعداد كاميرا ويب USB كجهاز الحصول على صورة الأصابع. لتحسين الصورة، يتم اختيار طريقة معادلة الرسم البياني (HE)بسبب الخوارزمية الأقل تعقيدًا، خاصة عند تقييم الأداء على منصة .FPGAتم اعتبار منصتي معالجة لإكمال الدراسة، وهما أجهزة الكمبيوتر المكتبية التي تستخدم برمجة MATLAB ومنصة .FPGA DE1-SoCتم إجراء مقارنة النتائج بين منصتي المعالجة هاتين، حيث وجد أن النتائج لكلا المنصتين أظهرت مخرجات متطابقة من حيث PSNR، والتي حققت قيمة 13.43 ديسيبل وMSE بقيمة 0.0454.

الكلمات المفتاحية: بصمة مفصل الإصبع (FKP)، FPGA، معادلة الرسم البياني (HE)، تحسين الصورة، Verilog HDL.